Area Efficient On-Chip Timeout Generator with Low Temperature and Low Supply Voltage Dependency

The present invention relates to electronic timing circuits, and more particularly to timeout generators.

Background of the Invention

Timeout functions are required in many applications, such as delayed reset functions. The timeout functions can be implemented by various means including pure analog means or combinations of analog and digital means. The analog implementations often require the charging and/or discharging of a capacitor that is compared against a voltage reference using a comparator. Conventional circuits typically use off-chip capacitors that are in the nanofarad range and large on-chip resistors in the megaohms range to provide timeout periods in the milliseconds range.

An appreciation of the present invention and its improvements can be obtained by reference to the accompanying drawings that are briefly summarized below, to the following detailed description of illustrated embodiments of the invention, and to the appended claims.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings.

FIG. 1 illustrates an example timeout generator (100) that is arranged in accordance with aspects of the present invention.

FIG. 2 is a timing diagram of an example timing generator operating in accordance with aspects of the present invention.

FIG. 3 is a schematic diagram of an example PTAT current source generator that is arranged in accordance with aspects of the present invention.

Detailed Description of the Preferred Embodiment

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, the invention is related to an area-efficient two-millisecond fully integrated BiCMOS analog time delay circuit with the time delay being temperature compensated and supply voltage independent. An ultralow PTAT current source comprises medium-value resistors to discharge an on-chip capacitor from a fixed zero-temperature coefficient voltage. The comparator monitors the capacitor voltage and changes stage from low to high when the capacitor is discharged below a reference voltage having a defined negative temperature coefficient. The negative temperature coefficient of the reference voltage and the positive temperature coefficient of the PTAT current source are such that the timeout period is independent of temperature to the first-order. The generated timeout delay is also independent of the

supply voltage and can be used with a supply voltage as low as two volts. For example, an on-chip capacitor in the picofarad range and a medium value resistor of approximately 50 Kohms can be used in accordance with the present invention to generate a two-second temperature compensated and supply voltage independent timeout function

An embodiment of the present invention uses analog components to generate timeout periods in the milliseconds range without requiring high values for on-chip components such as resistors or capacitors. For example, an embodiment comprising a 15 picofarad on-chip capacitor and a supply voltage of two volts can generate a timeout period in the millisecond range without using a resistor in the range of tens of Mohms. In contrast, conventional methods would require a current in the range of 10 nanoamps to achieve a timeout period in the millisecond range. To derive a 10nA discharge current would typically require an on-chip resistor of several Mohms.

FIG. 1 illustrates an example timeout generator (100) that is arranged in accordance with aspects of the present invention. Generator 100 comprises switch S1, comparator X1, current sources X2-X3, timing capacitor C1, and diode D1. Current source X2 is an ultralow current generator having a positive temperature coefficient and is capable of producing currents in the nanoamps range.

VREF1 is provided, for example, by a bandgap reference voltage generator, and has a temperature coefficient that is substantially zero. VREF2 is generated by applying a current (generated by current source X3) to a base-emitter junction provided by diode D1. VREF2 has a negative temperature coefficient in contrast to the positive temperature coefficient of current source X2. The offsetting temperature coefficients operate to maintain a temperature coefficient of the timeout period generated by generator 100 that is independent of temperature in the first-order.

In operation, switch S1 is initially closed and timing capacitor C1 is charged to VREF1. When switch S1 is opened, generator 100 starts generating the timeout period. Current source X2 generates a current of 5 nanoamps, which is used to discharge timing capacitor C1. Comparator X1 monitors the voltage of the timing

capacitor C1 and changes state from low to high when timing capacitor C1 discharges below VREF2.

FIG. 2 is a timing diagram of an example timing generator operating in accordance with aspects of the present invention. When switch S1 is opened, the voltage of timing capacitor C1 falls from VREF1 to below VREF2. When the voltage of timing capacitor C1 falls below VREF2, comparator X1 changes state from low to high. Timeout period t_0 is the period of time from the opening of switch S1 to the transition of comparator X1 from the low state to the high state.

Timeout period t_0 can be expressed as:

$$t_0 = \frac{C1 \times (VREF1 - VREF2)}{I_{out}} \qquad \text{(I)}$$

where VREF1 is equal to the bandgap reference voltage and VREF2 is equal to nVBE where n is equal to or less than unity.

In an exemplary embodiment using typical components, the timeout period t_0 can be expressed as:

$$t_0 = \frac{15pF \times (1.2V - 0.68V)}{4.5nA} = 1.7m\text{sec} \qquad \text{(II)}$$

where n is equal to unity.

FIG. 3 is a schematic diagram of an example PTAT current source generator that is arranged in accordance with aspects of the present invention. In an embodiment of the invention, generator 300 comprises current sources X2 and X3. As shown in the figure, generator 300 comprises P-channel device M4, which is configured to generate output current I_{PTAT}. Output current I_{PTAT} is applied to a node comprising a first terminal of resistor R31 and the emitter of NPN transistor Q31. The base of transistor Q31 is coupled to the base of transistor Q32 such that the transistors are biased equally. The collector of NPN transistor Q32 is arranged to provide output current I_{out}.

Current I_{out} is a function of resistors R31 and R32, the relative scaling of the NPN transistors, and the PMOS transistors of generator 300. Current I_{out} can be expressed as:

$$I_{out} = \frac{I_{PTAT}}{9^{(N-1)}} \quad \text{(III)}$$

where,

$$I_{PTAT} = \frac{VT \times \ln(9)}{R31} \quad \text{(IV)}$$

and,

$$N = \frac{R32}{R31} \quad \text{(V)}$$

From Equations III, IV, and V above and a scale factor of 3, output current I_{out} can be calculated as:

$$I_{out} = \frac{4.76\mu A}{1051} = 4.5nA$$

Accordingly, the total resistance used to produce an output current I_{out} of 4.5nA is around 62 kohms, which represents a substantial reduction over conventional methods for implementing on-chip resistors for generating relatively long-term timeout periods. Furthermore, the NPN current output of I_{out} can operate in the saturation region without affecting the IPTAT source due to the high I_{PTAT} / I_{out} ratio.

Various embodiments of the invention are possible without departing from the spirit and scope of the invention. In the example shown in Figure 3, the supply voltage variation of I_{out} is largely affected by the output impedance of P-channel transistor M4. However, a variety of conventional cascoded arrangements for the P-channel current source can be used to reduce supply voltage dependencies. While

PMOS transistor M1 is used for startup of the PTAT cell of generator 300, alternative start-up methods can be employed.

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.